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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,823	11/26/2003	Ernest S. Cohen	MSFT-2820/306478.1	9276

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EXAMINER	
SONG, JASMINE	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,823	COHEN, ERNEST S.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will; by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 22-28* is/are rejected.

7)☒ Claim(s) *20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/10/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

2. The drawings filed on 11/26/2003 have been approved by the Examiner.

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 3/10/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-17,23-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The language in claims 1, 11 and 23 "comparison of said counter's value with the recorded counter value (similar meaning of claims 11 and 23)" is not clear or distinct. It is not clear as to how the counter's value compare with the recorded counter value since the counter's value is the recorded counter value (from the claimed language). It is not possible from either the specification or the claims to determine the scope of this language or to determine the metes and bounds of the claims. Claims 2-10,12-17,24-28 are also rejected because they are depended on the rejection of claims 1, 11 and 23.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-6,9-10,18-19 and 22-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Zuraski Jr. et al., US 6510508 B1.

Regarding claims 1, Zuraski teaches that a method of clearing obsolete entries from a first one of a plurality of mapping caches (it is taught as one of TLBs, col.9, lines 37-38), each of the plurality of mapping caches being associated with a corresponding one of a plurality of processing units of a computing device (Zuraski teaches a computer system may be a multiprocessing computer system including additional processors), each of the caches being used to translate virtual addresses to physical addresses and storing mappings based on an address translation map, the method comprising:

maintaining a counter (it is taught as maintaining a base address register counter 405 to count the number of base address register tags, col.10, lines 51-53);

updating said counter (col.9, lines 46-47; base address register 301 may be updated during a context switch, that is, the number of base address register tags is updated since the base address register tag is associated with a base address register entry) each time the first one of the plurality of mapping caches is flushed (a context switch results in removal of all translations stored in the TLB, col.1, lines 44-45);

recording said counter's value in response to a change in the address translation map (it is taught as the new value of the register, col.11, lines 54-56);

determining the first one of the plurality of mapping caches has not definitely been flushed since said change in the address translation map occurred (it is taught as a match is found and a previously used address translation may be used again and no new tag need be assigned, col.11, lines 60-65 and col.2, lines 52-56) based on a comparison of said counter's value with the recorded counter value (col.11, lines 56-58); and

flushing the first one of the plurality of mapping caches (it is taught as no match is found and a TLB flush is needed, col.11, lines 58-60 and col.2, lines 52-56).

Regarding claim 2, Zuraski teaches that said counter is one of a plurality of counters, each counter being associated with a corresponding one of the mapping caches (since Zuraski teaches multiple TLBs, therefore, there are a plurality of counters associated with each TLB).

Regarding claim 3, Zuraski teaches that each of the plurality of counters is updated when a counter's corresponding mapping cache is flushed (it is taught as each of the plurality of counters is updated when there is a context switch).

Regarding claim 4, Zuraski teaches that the address translation map comprises links to pages of memory including a first page, and wherein said change comprises placing the address translation map in a state (it is taught as the LS-TLBInvalidateM signal may be used to indicate that the TLB is to be flushed) in which the address translation map does not contain any links to said first page (it is taught as a modification has occurred).

Regarding claims 5 and 6, Zuraski teaches that the address translation map defines portions of a memory that are readable or writeable by an entity, said portions of said memory including a first portion, and wherein said change comprises placing the

address translation map in a state in which said first portion is not readable or writable by said entity (it is taught as a flush of the TLB is occur only when certain conditions are met, col.12, lies 1-11).

Regarding claim 9, Zuraski teaches that further comprising: determining that an event has arisen that potentially makes use of the state of the address translation map prior to said change; wherein flushing the first one of the plurality of map caches is performed in response to the determination that said event has arisen (Fig.5, col.11, lines 66 to col.12, lines 17).

Regarding claim 10, Zuraski teaches that said event comprises a translation of a virtual address to a physical address that is contained in a portion of memory that was de-linked from the address translation map by said change (it is taught as turning off paging).

Regarding claim 18, Zuraski teaches that acomputer-readable medium having encoded thereon computer-executable instructions to perform a method of managing the flushing of a translation lookaside buffer that caches address mappings, the method comprising: receiving an access request that indicates a target location by virtual address and translating said virtual address to obtain a physical address of said target location (col.1, lines 33-41); comparing (1) a stored counter value associated with a page that comprises said target address (it is taught as maintaining a base address

register counter 405 to count the number of base address register tags, col.10, lines 51-53) with (2) a current counter value (it is taught as the new value of the register, col.11, lines 54-56); determining based on the comparison between said stored counter value and said current counter value(col.11, lines 56-58) that the translation lookaside buffer has not been flushed since an event affecting a mapping of said page has been modified (it is taught as a match is found and a previously used address translation may be used again and no new tag need be assigned, col.11, lines 60-65 and col.2, lines 52-56); and flushing the translation lookaside buffer (it is taught as no match is found and a TLB flush is needed, col.11, lines 58-60 and col.2, lines 52-56).

Regarding claim 19, Zuraski teaches that the address mappings are defined by an address translation map stored in a memory, the translation lookaside buffer caching mappings that are based on said address translation map (it is taught in col.1, lines 27-41).

Regarding claim 22, Zuraski teaches that an address translation control mechanism determines the membership of a set of pages of a memory that may be used to store portions of an address translation map, and wherein said event comprises a change in membership of said set (col.1, lines 46-49).

Regarding claim 23, Zuraski teaches that a method of clearing obsolete entries from a first one of a plurality of mapping caches(it is taught as one of TLBs, col.9, lines

37-38), each of the plurality of mapping caches being associated with a corresponding one of a plurality of processing units of a computing device (Zuraski teaches a computer system may be a multiprocessing computer system including additional processors), each of the caches being used to translate virtual addresses to physical addresses and storing mappings based on an address translation map, the method comprising: maintaining an object based on which the sequential progression of events can be determined (it is taught as maintaining a base address register counter 405 to count the number of base address register tags, col.10, lines 51-53); recording said object's value (it is taught as the new value of the register, col.11, lines 54-56) in response to a change to the address translation map (col.9, lines 46-47; base address register 301 may be updated during a context switch, that is, the number of base address register tags is updated since the base address register tag is associated with a base address register entry) that removes one or more of, (1) read access, or (2) read/write access, from a page (it is taught as receiving notification from load/store unit, col.10, lines 13-17); in response to a request to access said page, determining based on a comparison of said object's current value with the recorded value that the first one of the plurality of mapping caches has been flushed since said change occurred (col.11, lines 56-58); and if it cannot be determined with certainty based on said comparison that the first one of the plurality of mapping caches has been flushed since said change occurred (it is taught as a match is found and a previously used address translation may be used again and no new tag need be assigned, col.11, lines 60-65 and col.2, lines 52-56),

then flushing the first one of the plurality of mapping caches (it is taught as no match is found and a TLB flush is needed, col.11, lines 58-60 and col.2, lines 52-56).

flushing the first one of the plurality of mapping caches (it is taught as no match is found and a TLB flush is needed, col.11, lines 58-60 and col.2, lines 52-56).

Regarding claim 24, Zuraski teaches that said object comprises a clock (col.1, lines 22-29).

Regarding claims 25 and 26, Zuraski teaches that said object comprises a plurality of counters, each of the counters corresponding to one of the plurality of mapping caches, wherein each of the counters is incremented when the counter's corresponding mapping cache is flushed (col.10, lines 54-65, it is taught the counter may assert an overflow signal).

Regarding claim 27, Zuraski teaches that said change comprises removing read access to said page, and wherein said access request comprises a request to read said page (it is taught as TLB flush filter receive notification from load/store unit when a context switch occurs).

Regarding claim 28, Zuraski teaches that said change comprises removing read/write access to said page, and wherein said access request comprises a request

to write said page (it is taught as TLB flush filter receive notification from load/store unit when a context switch occurs).

Allowable Subject Matter

9. Claims 7-8 (except the rejections of 112 as shown above) and 20-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Willman et al	US 2003/0200402 A1
Masubuchi et al	US 6490657 B1

11. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

12. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song JS

Patent Examiner

November 22, 2005

FOR
Mano Padmanabhan

Supervisory Patent Examiner

Technology Center 2100

GARY PORTKA
PRIMARY EXAMINER